Design of an Optimum Switch Block for FPGA

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A field programmable gate array (FPGA) is a special type of integrated circuit that has contributed to the broaden application of electronics, from aerospace to defense, and from medical imaging to wireless communication. FPGA is useful because the internal switch blocks are reconfigurable even after manufacturing. However, FPGA is most useful if the internal switch blocks can be re-configured to satisfy large number of distinct cases. A switch block G with w terminals on each side is said to be a hyperuniversal switch block (HUSB), which boasts optimum routing ability if every set of nets satisfying the dimensional constraint (i.e., the number of nets on each side of G is at most w) is simultaneously routable through G. For efficiency reason, a switch block should contain as few switches as necessary. To date, the most efficient HUSB design has been shown by Fan with 6.3w number of switches. In this study, we designed an optimal hyperuniversal switch block with only 6w number of switches. We proved that 6w is the theoretical lower bound for HUSB. We further demonstrated how to obtain arbitrary sized (w) switch block from the proposed set of seven fundamental switch blocks, which are also HUSB. In comparison with other switch block designs, experimental results shows that our design is more switch efficient by 75.63% over the Disjoint switch block and by 4% over Fan's HUSB.