Generalized Decision Functions for Synthesis of Multi-level Logic Circuits Realized by Memristor Imply Gates

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The three passive circuit elements used in electrical engineering are the resistor, capacitor, and inductor. My research addresses the fourth fundamental element called the memristor. Memristors have a huge potential to realize logic circuits much more efficiently than CMOS circuits due to their power and size advantages. However, today's logic tools have been developed for CMOS circuits and do not take into account the unique properties of memristors. Memristors can remember the previous logic state until the next input is applied thus a memristor gate can be re-used repeatedly with timing pulses. An IMPLY gate is the basic Memristor gate, as opposed to AND/OR/NOT gates in traditional CMOS circuits. Series of IMPLY gates typically represent the state of a working memristor at successive timing pulses. My objective was to synthesize multi-level logic functions with memristor-realized IMPLY gates, and design the algorithms and software logic tools to create optimized memristor circuits. I used SOP, POS, ESOP and multi-level TANT networks to create a circuit optimized for memristor count and pulse count. In all these methods, there is a critical step to select the best essential prime implicant. I accomplished this using covering table (for Unate functions) and covering-closure table (for Binate functions), generating Decision Functions, and creating new algorithms to solve the Decision Functions. I implemented these algorithms in the software for the logic synthesis tools that I created. I also formulated a new Imply Sequence Diagram notation, which allows for visualization of the operation of a memristor circuit with sequence of pulses. My research lays a foundation for Electronic Design Automation of logic circuits for energy-efficient and compact devices.

Awards Won:

Second Award of $2,000