DIMOS: A Novel Low-Power, Fast Response Logic Gate Architecture

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At standard switching frequencies, short-circuit current is a leading cause of power dissipation in a complementary metal-oxide-semiconductor (CMOS) platform. Certain systems, such as mission-critical sensor nodes and implantable electronics, demand low power consumption and high reliability. Since the NOT gate (inverter) is a standard test bench for testing the effectiveness of CMOS power-saving measures, a novel inverter architecture with reduced short circuit current was explored. The proposed inverter architectures added in-series diode-connected MOSFETs, which dynamically limited short circuit current. These “diode-interrupter metal-oxide semiconductor” (DIMOS) architectures were evaluated with respect to each other and the standard CMOS configurations. For validation of the simulation models, a few DIMOS inverters were fabricated using a 0.5 um CMOS process available through MOSIS. It was found that the discrepancy between the models and experimental data increased with increasing frequency (due primarily to parasitic capacitance). The DIMOS architectures were evaluated in the context of a 3-bit flash analog-digital converter (ADC) for use in resource-constrained digitization schemes, such as in medical implants. The proposed ADC utilized DIMOS inverters in its thresholding scheme and featured novel DIMOS XOR gates. Furthermore, a computationally efficient optimization algorithm that sequentially performed lexicographic optimization and branch and bound was created to optimize FET dimensions for ADC components. Combined, these measures significantly lowered power consumption while maintaining the sampling speed necessary for medical implants.

Awards Won:

Second Award of $2,000

Samvid Education Foundation: Honorable Mention

National Security Agency Research Directorate : First Place Award "Future of Computing" of $1,000