Brain-Inspired Circuitry for the Future of AI and IoT: Optimizing the Analog Response of RRAMs under Pulsing for Synaptic Use

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On many pattern recognition and inference tasks the human brain, which consumes just 20W and occupies only 1.5L, can outperform AI running on large von Neumann (vN) systems. Closure of this efficiency gap will enable AI on IoT. Thus, intense research is underway on brain-inspired alternatives to vN, which capture the computationally-intensive parts of AI in massively parallel circuitry, interweaving computing and analog memory (synapse) elements. I optimize the analog response of resistive memories (RRAMs), for use as synapses in brain-inspired vN-alternatives. I studied non-filamentary (nf) RRAMs, because their conductance can be adjusted in a continuous fashion with voltage pulses applied between their 2 terminals. Key steps of my research: (a) Write a Kinetic Monte Carlo device simulator (KMC), capturing mixed ionic-electronic conduction central to nf-RRAM operation. Model conductance using nonlinear resistor network. (b) Use KMC to study RRAM response under different pulsing schemes. (c) Find pulsing schemes that yield the best synaptic response. (d) Benchmark system-level accuracy of my synaptic designs in NeuroSim, a neural network simulator. My contributions: (a) Developed physics-based KMC simulator in Python. (b) Validated KMC against published experimental data. (c) Using KMC characterized the synaptic behavior of nf-RRAMs under several pulsing schemes: standard, stepping, hybrid. (d) Standard pulsing yielded the poorest synaptic behavior. (e) Hybrid scheme yielded the most linear/symmetrical synaptic response. (f) Analyzed the system-level behavior of my synapses in NeuroSim. Conclusion: Using system level analysis, I showed that my hybrid scheme is nearly-ideal, yielding 90% learning accuracy, which is very close to the 93% rate achieved by the ideal synapse.

Awards Won:

Fourth Award of $500