Hybrid Graphene-Ferroelectric Devices Utilizing BaTiO3 - SrTiO3 Superlattices

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I successfully integrated graphene onto a BaTiO 3 /SrTiO 3 (BTO/STO) ferroelectric superlattice to create a graphene-ferroelectric field effect transistor (GFFET). I achieved ferroelectricity-induced gating hysteresis across the graphene channel at 70K. At room temperature we observed anti-hysteresis which we attribute to the presence of charge traps at the graphene-ferroelectric interface. Tuning the ratio of BTO to STO to reduce intrinsic anomalies at the superlattice surface, and depositing graphene at a high temperature to minimize surface contaminants, reduced the number of charge traps. We characterize charge trapping dependence upon temperature and upon applied gate voltage range and ramp speed for this transistor. With further superlattice tuning and improved graphene deposition, hysteresis may be achievable at room temperature. Graphene-ferroelectric hybrid transistor devices with reliable gating hysteresis at room temperature could be used for non-volatile memory applications. These devices could provide an excellent alternative to the current silicon-based transistors.

Awards Won:
Second Award of $2,000