Fault-Tolerant Arithmetic Computing using Partial Triple Modular Redundancy (PTMR)

Parhi, Rahul

Integrated circuits fabricated using nano-scale CMOS technologies are prone to errors because of fluctuations in threshold voltage and supply voltage, electromigration, random dopant fluctuations, aging, timing errors and soft errors. Design of nano-scale failure-resistant systems has drawn significant interest in past few years. This project explores design of fault-tolerant arithmetic computing systems. Five new fault-tolerant adders are proposed and the fault tolerance levels of these adders are compared with that of the conventional triple modular redundancy (TMR) adder. Bit-level computer simulations are carried out to compute signal-to-error ratio for different computational logic and voting circuit fault rates and for different word-lengths, using 10 million Monte-Carlo experiments. This paper demonstrates that the proposed novel partial triple modular redundancy (Partial TMR or PTMR) approach achieves the same or better fault-tolerance as that of conventional TMR but with significantly less hardware overhead. It is shown that the hardware overhead can be reduced by 75% to 87.5% with P = 4 as the word-length varies from 16 to 32, with average error power equal to or less than that of conventional TMR. It is shown that P = 3 or 4 is sufficient for word-lengths varying from 16 to 32. The key contributions include: fault-tolerant arithmetic computing analysis for the first time, analysis of effect of voting circuit error for the first time, and proof that PTMR is more fault-tolerant while requiring significantly less hardware overhead. The proposed approach can avoid catastrophic situations in signal processing, embedded systems, storage, security, deep-space, biomedical, automobile, and military applications.

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