An Iterative Model for Developing Network-on-Chip (NoC) Architectures

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Since the recent birth of the Network-On-Chip (NoC) paradigm for simulating System-On-Chip activity, various topological and routing models have been presented to advance processing technologies. The search for the most effective solution revolves around three major goals: low latency (packet travel time), high throughput (relative measure of packet traffic reaching destination), and minimal cost (a function of wire, or connection, length). The purpose of this study is to propose a novel prototype for designing NoCs using an intuitive method relevant to the NoC community for its revolutionary outlook on optimization techniques. The basic premise of this model is to incorporate the main function of NoCs, i.e. processing packet traffic, in the actual design of these networks. Using a simple formula weighing traffic and preferential attachment (an evaluator used in developing scale-free networks) probabilities, this model allows for a variety of networks with distinctive characteristics to evolve iteratively based on the initial condition, weight. Analysis of these networks reveal low latency is best achieved when traffic and preferential attachment are in balance, while high throughput results from networks developed with a special focus on traffic (as is to be expected). Additionally, a comparison with the standard mesh grid suggests the model performs just as well as mesh networks in some cases and better in many other areas. This paradigm is beneficial for furthering the current understanding of complex NoCs and advancing emerging technologies.

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