Optimizing Micro-Computer Architecture in the Arithmetic Logic Unit

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Computer processing speed has historically followed a trend of exponential improvement. This phenomenon is explained by Moore’s Law, which states that the number of transistors in a microchip doubles every few years. As the size of transistors decreases, computers become faster and consume less energy. However, transistors are approaching their physical size limit, requiring a new method to improve processing speed. Rather than making the pieces inside the computer smaller, this project optimizes the bit arithmetic algorithms defining processing speed by combining two critical operations in the Arithmetic Logic Unit (ALU), the multiplication and division circuits. Developing the combinational circuit relies on combining the designs of the multiplication and division circuits. Since contemporary multipliers and standard division circuits rely on an adding or subtracting iterative design, many fundamental processes repeat. Innovating an adder/subtractor as the axis of the combinational circuit combines these procedures. The adder/subtractor includes a combination of the CSA and the Two’s Complement, which turns bits negative, so the circuit can add and subtract. The K-value is a single bit acting as the operation code for the demultiplexers to sort through bit pathways and a bit switch for the entire circuit. Modeling the combo circuit in a digital logic simulator, the truth tables for the outputs exactly match the respective multiplication and division solutions. Both operations’ bit pathways overlap significantly, saving the space two circuits would require by replacing dozens of single adders and subtractors with easily switchable functions by 15%. By expanding combinational circuits to encompass more arithmetic functions, the CPU can become substantially faster.

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