Designing a Novel Vertically-Stacked Nanowire-Based Complementary Field-Effect Transistor for Low-Power Applications

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Physical limitations behind conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) have prevented device miniaturization by increasing leakage current and consequently, power consumption. Many device modifications have been proposed to address these physical limitations and allow for continued down-scaling. One of the proposed devices for overcoming the aforementioned physical limitations is the gate-all-around FET (GAAFET), which semiconductor technology is currently adopting because of its excellent gate controllability and compatibility with existing fabrication processes. Firstly, technology computer-aided design (TCAD) simulations were used to optimize the source and drain doping concentrations, metal gate work function, and gate oxide dielectric constant of a cuboid silicon gate-all-around (GAA) nanowire nMOSFET. Next, the nanowire diameter was reduced from 15 to 10, 7, 5, and 3 nanometers while keeping the source and drain doping concentration and work function constant. Different dielectric constants were also tested at these narrow diameters while activating quantum mechanical effects. Vertically stacked nanowires were studied to improve the on-current without increasing the area occupied by the device. Furthermore, vertically stacked nanowires can lead to the development of a Complementary Field-Effect Transistor (CFET) device, where an NMOS and PMOS pair are stacked vertically on each other instead of side by side in a conventional CMOS implementation. 3-nm nanowire FETs are an excellent contender for use in low-power electronics because of their extremely low leakage current and small occupied area. By developing a novel, low-power CFET device, we can continue extending our electronics' battery life and lowering our electricity usage.

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