CryoFlow: A Streaming FPGA Architecture for High-Efficiency Cryogenic Electron Microscopy Reconstruction

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Cryogenic Electron Microscopy (Cryo-EM) is the cornerstone technique for determining atomic-resolution structures of proteins implicated in neurodegenerative diseases like Alzheimer's. However, processing the millions of noisy images generated per session requires multi-GPU supercomputers costing upward of $30,000. Current GPU-based pipelines suffer from systemic inefficiencies: the PCIe data-transfer bottleneck and precision redundancy from 32-bit floating-point arithmetic that computes biological noise rather than signal. This project engineered CryoFlow, a domain-specific hardware accelerator implemented on an AMD Xilinx Kria SoC FPGA. A zero-copy Unified Memory Architecture was implemented in Rust via the Xilinx Runtime (XRT), eliminating PCIe bottlenecks. The likelihood-scoring algorithm was refactored to Fourier space and quantised to 8-bit integers, matched precisely to the biological noise floor. A custom Vitis HLS dataflow pipeline featuring a 256-way SIMD DSP array achieved 153.6 Giga-MACs, with reference projections cached in on-chip UltraRAM to eliminate external bandwidth costs. Validated against 30 diverse EMPIAR datasets, CryoFlow achieved 4.4 Joules per 1,000 particles, an 8.6-fold energy efficiency improvement over a 315W flagship GPU. By shifting the computational paradigm from general-purpose GPUs to application-specific silicon, CryoFlow offers a low-cost, scalable solution that can democratise high-performance structure determination for biomedical research laboratories worldwide.

Awards Won:
Second Award of $2,400
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