A Novel Hybrid Equalization Technique for High-Speed Data Communications

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As computing power increases, faster wireline data communication speeds are required, going from today's 128GT/s to next-generation 256GT/s. With increasing data-rates through circuit boards, there is more symbol degradation in electrical signals: (1) Inter-Symbol-Interference errors blurring symbols together creating linear errors and (2) crosstalk from parallel channels, creating nonlinear errors. Equalizers reduce corroded symbols by boosting energy at the critical signal frequency. Traditional Decision-Feedback-Equalizers (DFEs) work at current data-rates but require a minimum 13 ps/sym. At 256GT/s, the time is 7.5 ps/sym, making DFEs unusable for next-generation. This project creates next-gen equalizers to allow for 256GT/s data-rates. Two options are created. First, a Maximum-Likelihood-Sequence-Estimation (MLSE) which avoids the timing penalties of DFEs by pre-determining possible data options. MLSE performs better than DFE but has drawbacks: (1) faster data-rates require more symbol history, growing algorithm-complexity exponentially and (2) it cannot combat nonlinear (crosstalk) errors. Therefore, a novel hybrid equalizer was conceptualized, designed, coded, and implemented for improved error reduction, allowing faster data-rates. A Feed-Forward-Equalizer (FFE) was combined with a small 2-layer 4-node neural network (ML). The novel Hybrid FFE-ML equalizer shows up to 100x better performance in error-rate, improving both linear ISI and nonlinear crosstalk errors, and was validated for hardware implementation via a Field-Programmable-Gate-Array. With improved error-rates, the novel Hybrid FFE-ML equalizer can deliver (1) 30-50% higher data-rates with greater data packaging in current frequency standards and (2) 2x higher data-rates for next-gen 256GT/s.

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